A PROCEDURE FOR TESTING FOR REALIZABILITY AND THE REALIZATION OF A CIRCUIT MATRIX

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THESIS

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ABSTRACT

Several procedures for the realization of a given realizable circuit matrix are reviewed and the techniques discussed. A new method for the realization of a given circuit matrix is introduced. The procedure also introduces a positive test to determine if the given matrix is realizable as a circuit matrix.

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INTRODUCTION

The problems of realizability and realization of a given circuit matrix have been drawing attention for a long time. The importance of these problems lie, mainly, in their wide application to the synthesis of complex modern day electrical networks, communication nets, and switching circuits.

The problem of realizability is that of determining if a graph exists that can be described by a given circuit matrix. The problem of realization is finding the graph that corresponds to a given circuit matrix.

There have been many attacks on the problem of realization of a given circuit matrix. Seshu (1) claimed that if an incidence matrix can be found through the relation that the product of the incidence matrix and the transpose of the circuit matrix is empty, the problem of realization of a given circuit matrix is solved. Parker and Loshe (2) have presented a procedure to synthesize a graph from a given realizable fundamental circuit matrix. Fu (3) has presented a method for the realization of any given realizable circuit through the realization of the fundamental circuit matrix. Ash and Kim (4) have worked out a synthesis procedure applicable to a restricted class of circuit matrices with a list of submatrices that are not realizable.

The answers to the problem of realizability of a given circuit matrix leave much to be desired. This paper attacks both problems simultaneously through tests for realizability and the realization of subgraphs and the connection of these subgraphs.

DISCUSSION OF EXISTING REALIZATION TECHNIQUES

2.1 Combinatorial Approach

Parker and Loshe (2) attack the problem of realization of a given realizable fundamental circuit matrix by partitioning the given fundamental circuit matrix as follows:

$B_f = (U:F_t:F_m:F_1)$

Where U is a unit matrix, F_1 is a submatrix of the tree with only one nonzero entry in each column, F_t is the submatrix with the maximum number of nonzero entries in one row and F_m is the submatrix consisting of the remaining columns of B_f. The concept of "unique connections" is introduced and for cases in which this concept can be used, the problem of realization is greatly reduced.

For example consider the fundamental circuit matrices B_{f1} and B_{f2}, that correspond to the same graph:

B_{f1} =

c	e	f	h	a	b	d	g
1	0	0	0	1	1	1	0
0	1	0	0	0	1	0	1
0	0	1	0	1	1	0	1
0	0	0	1	0	0	1	1

B_{f2} =

a	b	c	d	e	f	g	h
1	0	0	0	1	1	0	0
0	1	0	0	1	0	1	0
0	0	1	0	0	1	0	1
0	0	0	1	0	0	1	1

For B_{f1}, F_t can consist of columns a, b, and d. Applying the rules set forth, there is a trunk chain a - b - d established with the tree completed with the unique connection of main branch g at the junction of b and d. In the case of B_{f2}, F_t can consist of any two of the columns, e, f, g, and h. The concept of unique connection does not hold and the matrix can be realized only through

applying the principle that each row consists of a linear path with the ends connected by a link.

2.2 Growing a Graph Using Constricted Matrices

Fu (3) presented a method for the realization of any given realizable circuit matrix through the realization of a fundamental circuit matrix $B_f = (U:E)$, where the submatrix U corresponds to the chords of some tree of the realized graph and E is a submatrix that corresponds to the branches of this tree. The realization of B_f is accomplished through a step by step realization of a series of its constricted matrices. A constricted circuit matrix of a circuit matrix B_f is defined as a submatrix of B_f which contains all columns of U and some of the columns of E.

This seems to be a straight forward approach to the problem, however, it is sometimes possible to add a branch to the tree in more than one location. This requires one to carry forward all possible subgraphs in order to insure the realization.

2.3 Realization of a Graph Containing a Maximal Path

Ash and Kim (4) worked out a systematic procedure to realize a realizable circuit matrix for any matrix whose tree forms a maximal path. If the columns of the tree are arranged so that no two 1's are separated by one or more 0's, then the edges of the tree taken in the order that they appear in the matrix will form a maximal path of the graph and the graph is realized. There are six submatrices listed that are not realizable.

2.4 Summary of Deficiencies of Existing Methods

All of the methods discussed above have one or more of the following deficiencies:

a) No positive test for realizability.

b) No method for selecting the tree most easily realizable.

DEFINITIONS

3.1 Introduction

Some technical terms will be defined here for added emphasis. All other technical terms can be found in Seshu and Reed (5).

Definition 1: DEGREE OF A VERTEX. The degree of a vertex is the number of edges incident at the vertex.

Definition 2: PATH. A path is an open edge train in which the terminal vertices are of degree 1 and each other vertex is of degree 2.
(The degree of the vertex is with respect to the path and not the entire graph.)

Definition 3: MAXIMAL PATH. A maximal path is a path which includes all vertices of the graph. A maximal path is a tree of the graph.

Definition 4: NONMAXIMAL PATH. A nonmaximal path is a path that does not include all vertices of the graph.

Definition 5: CIRCUIT. A circuit is a closed edge train in which the degree of each vertex is two. (The degree of the vertex is with respect to the circuit and not the entire graph.)

Definition 6: HAMILTON CIRCUIT. A Hamilton circuit is a circuit which includes all vertices of the graph. A Hamilton circuit contains a maximal path and hence a tree of the graph.

Definition 7: EDGE-DISJOINT UNION OF CIRCUITS. An edge-disjoint union of circuits is a union of two or more circuits no two of which have a common edge.

Definition 8: THE CIRCUIT MATRIX, B_a. $B_a = (b_{ij})$ contains one row

for each circuit of the graph and one column for each edge, and

b_{ij} = 1 if edge j is in circuit i

b_{ij} = 0 if edge j is not in circuit i.

Definition 9: SERIES EDGES. Two edges are in series if they have exactly one common vertex and that vertex is of degree 2. Two edges are in series if each circuit that contains one of them also contains the other.

Definition 10: PARALLEL EDGES. Two edges are in parallel if they are incident at the same pair of vertices. Two edges that are in parallel form a two edge circuit.

Definition 11: SERIES COMBINATION. To combine two edges that are in series, replace the two edges with a single edge. This operation will reduce the number of edges and the number of vertices by one.

Definition 12: PARALLEL COMBINATION. To combine two edges that are in parallel, replace the two edges with a single edge. This operation will reduce the number of edges by one, but will not change the number of vertices.

Definition 13: THE REDUCED CIRCUIT MATRIX, B_{ar}. The reduced circuit matrix is the residue of the circuit matrix after repeated series combinations and parallel combinations have eliminated all series edges and parallel edges.

THEOREMS, LEMMAS, COROLLARIES, AND CONJECTURES

4.1 Introduction

The following theorems, lemmas, corollaries and conjectures included here will be used in the tests for realizability and the realization of a given circuit matrix.

Theorem 1: MINIMUM NUMBER OF EDGES. The minimum number of edges required for a graph with each vertex of degree 3 is given by:

$e_{min} = \frac{v \times 3}{2}$ for v even, and

$e_{min} = \frac{(v \times 3) + 1}{2}$ for v odd.

Proof: Consider the value of an edge incident to a vertex to be one-half, that is one-half of the edge belongs to each of its vertices. Then the number of edges drawn from a vertex is equal to one-half the degree of the vertex.

a) If v is even and all vertices are of degree 3, then $e_{min} = (1/2)(3 \times v)$.

b) Since a half edge is not permitted in the graph, for v odd, one vertex must be of degree 4. From Lemma 2-1 (5), in any finite graph, there is an even number of vertices of odd degree.

$$e_{min} = (1/2)3(v-1) + (1/2)4 = (1/2)(3v + 1).$$

Lemma 1. The maximum number of edges possible in a graph that contains no parrallel edges is given by:

$$e_{max} = \frac{v(v - 1)}{2}$$

Theorem 2: A REALIZABILITY THEOREM. If the graph contains a maximal path and this maximal path is chosen to be the tree, then necessary and sufficient condition for the circuit matrix to be realizable is

that the columns of the tree can be arranged so that no two 1's are seperated by one or more 0's in any independent row.

Proof: Since the tree is a maximal path, the columns of the tree can be arranged in the order that they appear as the path is transversed. With the columns so arranged, any nonmaximal path which is a proper subset of this tree, must form a row of 1's, otherwise there would be two or more nonmaximal paths. The independent rows of the matrix have one edge each that is not in the tree, therefore, if the edges in the tree do not form a single path, the remaining edge can not form a circuit of the graph.

Corollary 1: REALIZABILITY OF GRAPH WITH HAMILTON CIRCUIT. If (v - 1) edges of the Hamilton circuit are chosen as the branches of the tree, then necessary and sufficient condition for the realization of the circuit matrix is that the columns of the tree can be arranged so that no two 1's are seperated by one or more 0's in any independent row of the matrix.

Proof: Since (v - 1) edges of a Hamilton circuit is a maximal path of the graph, the corollary is proven by Theorem 2.

Conjecture 1: SUBMATRICES NOT REALIZABLE. It is not possible to arrange the columns of the following submatrices so that no two 1's are seperated by one or more 0's.

a)
$$\begin{matrix} 1 & 1 & 0 \\ 1 & 0 & 1 \\ 0 & 1 & 1 \end{matrix}$$

b)
$$\begin{matrix} 1 & 1 & 0 & 0 \\ 0 & 1 & 1 & 0 \\ 0 & 1 & 0 & 1 \end{matrix}$$

If the columns of the tree consisting of a maximal path can be so arranged so that either of these

submatrices is a submatrix of the columns of the tree, then the circuit matrix is not realizable.

PROCEDURES FOR TESTING FOR REALIZABILITY AND THE REALIZATION OF A GIVEN CIRCUIT MATRIX

5.1 Introduction

The only graphs that will be considered are non-oriented, non-separable, and planar. No generalization is lost if series combination and parallel combination are used, provided the edges and vertices that are removed are reinserted in the final graph.

The method used to obtain the realization of the graph is to break the graph into subgraphs that contain Hamilton circuits. The submatrices corresponding to these subgraphs are tested for realizability and, if realizable, the subgraphs are realized. The subgraphs are tested on a step by step basis to determine if it is possible to combine them and if the combination is possible, the graph is realized.

5.2 Procedure

The procedure outlined below is designed for hand calculation. The procedure will be given in a step by step order.

Step 1. Determination of the number of vertices

A set of independent rows are obtained from a given circuit matrix by Jordan's elimination method. The number of vertices in the graph is determined from this set of independent rows by the relation $v = e - b + 1$. Where v is the number of vertices, e is the number of edges, and b is the number of independent rows.

Step 2. Obtaining the Reduced Circuit Matrix, B_{ar}.

Generate all possible circuits by modulo-2 addition of all combinations of the independent rows. Eliminate all edge-disjoint unions of circuits. Use series combination and parallel combination to

eliminate all series and parallel edges. The residue of this operation is B_{ar}.

Step 3. The First Subgraph

a. The Hamilton Circuit

Select a row of B_{ar} with the largest number of non-zero entries. This is a Hamilton circuit of some subgraph.

b. Selection of the tree of the first subgraph

Use all except one of the edges of this Hamilton circuit as the tree of this subgraph. If this Hamilton circuit has v edges, this will be a tree of the graph.

c. Completing the Submatrix

Select all rows of B_{ar} that have exactly one edge not contained in the tree. Form a submatrix of these rows.

d. Test for Realizability and the Realization of the First Subgraph

Arrange the columns of the tree of this submatrix so that no two 1's are separated by one or more 0's in any row of this submatrix. If this is not possible, it will be possible to obtain one of the configurations of Conjecture 1. and the subgraph will not be realizable.

e. Deletion of Rows of B_{ar}.

Delete all rows of B_{ar} that contain a chord of the tree in the subgraph that has been realized.

Step 4. The Second Subgraph

a. The Hamilton Circuit

Select a row of B_{ar} with the largest number of nonzero entries that has at least two edges in common with the tree of the subgraph that has been realized. This is a Hamilton circuit of some subgraph.

b. Selection of the tree for the second subgraph

Use all except one of the edges of this Hamilton circuit as the tree of the second subgraph.

c. Completing the Submatrix.

Select all rows of B_{ar} that have exactly one edge not contained in the tree. Form a submatrix of these rows.

d. Test for Realizability and the Realization of the Second Subgraph.

Arrange the columns of the tree of this submatrix so that no two 1's are separated by one or more 0's in any row of this submatrix. If this is not possible, it will be possible to obtain one of the configurations of Conjecture 1 and the subgraph will not be realizable.

e. Joining the Subgraphs

If the graph is realizable, it must be possible to arrange the columns of the common edges so that they appear in the same order in both submatrices.

f. Deletion of rows of B_{ar}

Delete all rows of B_{ar} that contain a chord of the tree in the subgraph that has been realized.

g. Configuration of the Partial Tree

When the subgraphs are joined, there are three possible configurations of the tree, or partial tree, thus far obtained.

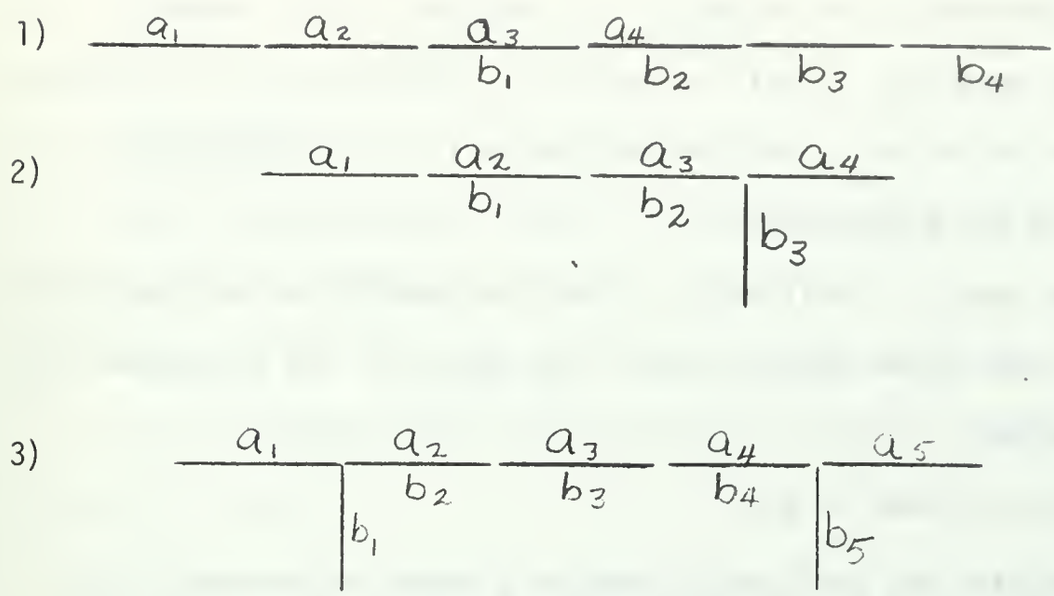

Fig. 1

For case 1, all columns contained in both trees can be arranged so that no two 1's are separated by one or more 0's in any row when the columns of the second submatrix are placed adjacent to the columns of the first. For cases 2 and 3, the tree configuration must be carried forward.

Step 5 Subsequent Subgraphs

a. The Hamilton Circuit

Select a row of B_{ar} with the largest number of non-zero entries that has at least two edges in common with a path in the partial tree obtained above. This is a Hamilton circuit of some subgraph.

b. Selection of the Tree for Subsequent Subgraphs

Use all except one of the edges of the Hamilton circuit as the tree of this subgraph.

c. Completing the Subgraph

Select all rows of B_{ar} that have exactly one edge not contained in the tree. Form a submatrix of these rows.

d. Test for Realizability and the Realization of Subsequent Subgraphs

Arrange the columns of the tree of this submatrix so that no two

1's are separated by one or more 0's in any row of this submatrix. If this is not possible, it will be possible to obtain one of the configurations of Conjecture 1 and the subgraph will not be realizable.

e. Joining the Subgraphs

If the graph is realizable, it must be possible to arrange the columns of the common edges so that they appear in the same order in each submatrix.

f. Deletion of Rows of B_{ar}

Delete all rows of B_{ar} that contain a chord of the tree in the subgraph that has been realized.

g. Configuration of the Partial Tree

There will be three possible configurations for the tree, or partial tree, obtained when the edges of the tree of this subgraph are joined to the partial tree obtained above.

Step 6 Realization of the Graph

a. Realization of the Reduced Circuit Matrix

Repeat the procedure outlined in Step 5 until there are no rows left in B_{ar}. At this point, there will be v - 1 edges in the tree and the realization is complete.

b. Reinsertion of Series and Parallel edges.

The graph is completed by reinserting the series and parallel edges that were removed in Step 2.

ILLUSTRATIVE EXAMPLES

6.1 Introduction

The following examples serve to illustrate the procedures that have been outlined above.

6.2 Example 1

In this example, there are no series or parallel edges and B_{ar} is given in Fig. 2.

Select row 6 as a Hamilton circuit for the first subgraph. The tree for this subgraph is chosen to be edges 3, 9, 10, 14, and 16. The rows of B_{ar} that have exactly one edge not contained in this tree are 6, 29, 51, 105, and 106. This submatrix can be put into the following form:

	a	b	d	m	o	i	n	p	j	c
6	1	0	0	0	0	1	1	1	1	1
29	0	1	0	0	0	0	1	1	1	1
51	0	0	1	0	0	0	0	0	1	1
105	0	0	0	1	0	1	1	0	0	0
106	0	0	0	0	1	0	0	1	1	0

It is seen that this submatrix meets the criterion for realizability and the tree is a path of the subgraph consisting of the edges i, n, p, j, and c in that order. After the rows of B_{ar} containing one or more chords of this tree have been deleted, the following rows remain in B_{ar}. 54, 56, 58, 60, 62, 64, 66, 68, 107, 108, and 85 through 104.

	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p	q	r	s	t
1	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
2	1	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0
3	1	0	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0
4	1	0	1	0	0	0	0	0	1	0	0	0	0	1	1	0	0	0	0	0
5	1	0	1	0	0	0	0	0	0	1	0	0	1	0	0	1	0	0	0	0
6	1	0	1	0	0	0	0	0	1	1	0	0	0	1	0	1	0	0	0	0
7	1	0	0	1	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0
8	1	0	0	1	0	0	0	0	1	0	0	0	0	1	0	1	0	0	0	0
9	1	0	0	1	0	0	0	0	0	1	0	0	1	0	1	0	0	0	0	0
10	1	0	0	1	0	0	0	0	1	1	0	0	0	1	1	0	0	0	0	0
11	1	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0
12	1	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	1	0	0	0
13	1	0	0	0	1	0	0	0	0	0	1	0	1	0	0	0	0	1	0	0
14	1	0	0	0	1	0	0	0	1	0	1	0	0	1	0	0	0	1	0	0
15	1	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	1	0	0
16	1	0	0	0	0	1	0	0	1	0	0	0	0	1	0	0	0	1	0	0
17	1	0	0	0	0	1	0	0	0	0	1	0	1	0	0	0	1	0	0	0
18	1	0	0	0	0	1	0	0	1	0	1	0	0	1	0	0	1	0	0	0
19	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0
20	1	0	0	0	0	0	1	0	1	0	0	0	0	1	0	0	0	0	1	0
21	1	0	0	0	0	0	1	0	0	0	0	1	1	0	0	0	0	0	0	1
22	1	0	0	0	0	0	1	0	1	0	0	1	0	1	0	0	0	0	0	1
23	1	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	1
24	1	0	0	0	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1
25	1	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0	0	0	1	0
26	1	0	0	0	0	0	0	1	1	0	0	1	0	1	0	0	0	0	1	0

FIGURE 2

	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p	q	r	s	t
27	0	1	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
28	0	1	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0
29	0	1	1	0	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0
30	0	1	1	0	0	0	0	0	1	1	0	0	1	0	0	1	0	0	0	0
31	0	1	0	1	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0
32	0	1	0	1	0	0	0	0	1	0	0	0	1	0	0	1	0	0	0	0
33	0	1	0	1	0	0	0	0	0	1	0	0	0	1	1	0	0	0	0	0
34	0	1	0	1	0	0	0	0	1	1	0	0	1	0	1	0	0	0	0	0
35	0	1	0	0	1	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0
36	0	1	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0
37	0	1	0	0	1	0	0	0	0	0	1	0	0	1	0	0	0	1	0	0
38	0	1	0	0	1	0	0	0	1	0	1	0	1	0	0	0	0	1	0	0
39	0	1	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	1	0	0
40	0	1	0	0	0	1	0	0	1	0	0	0	1	0	0	0	0	1	0	0
41	0	1	0	0	0	1	0	0	0	0	1	0	0	1	0	0	1	0	0	0
42	0	1	0	0	0	1	0	0	1	0	1	0	1	0	0	0	1	0	0	0
43	0	1	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	1	0
44	0	1	0	0	0	0	1	0	1	0	0	0	1	0	0	0	0	0	1	0
45	0	1	0	0	0	0	1	0	0	0	0	1	0	1	0	0	0	0	0	1
46	0	1	0	0	0	0	1	0	1	0	0	1	1	0	0	0	0	0	0	1
47	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	1	0
48	0	1	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0	0	1	0
49	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	1
50	0	1	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	1
51	0	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p	q	r	s	t
52	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0
53	0	0	1	0	1	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0
54	0	0	1	0	1	0	0	0	0	1	0	0	0	0	0	1	1	0	0	0
55	0	0	1	0	1	0	0	0	0	0	1	0	0	0	1	0	0	1	0	0
56	0	0	1	0	1	0	0	0	0	1	0	0	0	0	0	1	0	1	0	0
57	0	0	1	0	0	1	0	0	0	0	0	0	0	0	1	0	0	1	0	0
58	0	0	1	0	0	1	0	0	0	1	0	0	0	0	0	1	0	1	0	0
59	0	0	1	0	0	1	0	0	0	0	1	0	0	0	1	0	1	0	0	0
60	0	0	1	0	0	1	0	0	0	1	1	0	0	0	0	1	1	0	0	0
61	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	1	0
62	0	0	1	0	0	0	1	0	0	1	0	0	0	0	0	1	0	0	1	0
63	0	0	1	0	0	0	1	0	0	0	0	1	0	0	1	0	0	0	0	1
64	0	0	1	0	0	0	1	0	0	1	0	1	0	0	0	1	0	0	0	1
65	0	0	1	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	1
66	0	0	1	0	0	0	0	1	0	1	0	0	0	0	0	1	0	0	0	1
67	0	0	1	0	0	0	0	1	0	0	0	1	0	0	1	0	0	0	1	0
68	0	0	1	0	0	0	0	1	0	1	0	1	0	0	0	1	0	0	1	0
69	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0
70	0	0	0	1	1	0	0	0	0	1	0	0	0	0	1	0	1	0	0	0
71	0	0	0	1	1	0	0	0	0	0	1	0	0	0	0	1	0	1	0	0
72	0	0	0	1	1	0	0	0	0	1	1	0	0	0	1	0	0	1	0	0
73	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	1	0	1	0	0
74	0	0	0	1	0	1	0	0	0	1	0	0	0	0	1	0	0	1	0	0
75	0	0	0	1	0	1	0	0	0	0	1	0	0	0	0	1	1	0	0	0
76	0	0	0	1	0	1	0	0	0	1	1	0	0	0	1	0	1	0	0	0

	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p	q	r	s	t
77	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	1	0	0	1	0
78	0	0	0	1	0	0	1	0	0	1	0	0	0	0	1	0	0	0	1	0
79	0	0	0	1	0	0	1	0	0	0	0	1	0	0	0	1	0	0	0	1
80	0	0	0	1	0	0	1	0	0	1	0	1	0	0	1	0	0	0	0	1
81	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	1
82	0	0	0	1	0	0	0	1	0	1	0	0	0	0	1	0	0	0	0	1
83	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	1	0
84	0	0	0	1	0	0	0	1	0	1	0	1	0	0	1	0	0	0	1	0
85	0	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0
86	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0
87	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	1	0	1	0
88	0	0	0	0	1	0	1	0	0	0	1	0	0	0	0	0	0	1	1	0
89	0	0	0	0	1	0	1	0	0	0	0	1	0	0	0	0	1	0	0	1
90	0	0	0	0	1	0	1	0	0	0	1	1	0	0	0	0	0	1	0	1
91	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	1	0	0	1
92	0	0	0	0	1	0	0	1	0	0	1	0	0	0	0	0	0	1	0	1
93	0	0	0	0	1	0	0	1	0	0	0	1	0	0	0	0	1	0	1	0
94	0	0	0	0	1	0	0	1	0	0	1	1	0	0	0	0	0	1	1	0
95	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	1	0
96	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0	0	1	0	1	0
97	0	0	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	0	1
98	0	0	0	0	0	1	1	0	0	0	1	1	0	0	0	0	1	0	0	1
99	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	1	0	1
100	0	0	0	0	0	1	0	1	0	0	1	0	0	0	0	0	1	0	0	1
101	0	0	0	0	0	1	0	1	0	0	0	1	0	0	0	0	0	1	1	0
102	0	0	0	0	0	1	0	1	0	0	1	1	0	0	0	0	1	0	1	0

	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p	q	r	s	t
103	0	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0
104	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	1
105	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0	0	0	0
106	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	0	0	0
107	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	0	0
108	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1

Select row 56 to be a Hamilton circuit of the second subgraph. Note that this row has edges j, c, and p in common with the first subgraph. Chose edges j, c, p, r, and k to be the tree of this subgraph. The rows of B_{ar} that have exactly one edge not in this tree are 56, 58, and 107. This submatrix can be put in the form:

	e	f	q	p	j	c	r	k
56	1	0	0	1	1	1	1	1
58	0	1	0	1	1	1	1	0
107	0	0	1	0	0	0	1	1

It is seen that this submatrix meets the criterion for realizability and the tree is a path of the subgraph consisting of edges p, j, c, r, and k in that order. It is also noted that the order of the edges common to both subgraphs is the same. Since the common edges are on the ends of the paths in both subgraphs, the partial tree obtained when the two subgraphs are joined will be a path. The submatrix for the combination of the first two subgraphs can be put into the following form:

	a	b	d	m	o	e	f	q	i	n	p	j	c	r	k
6	1	0	0	0	0	0	0	0	1	1	1	1	1	0	0
29	0	1	0	0	0	0	0	0	0	1	1	1	1	0	0
51	0	0	1	0	0	0	0	0	0	0	0	1	1	0	0
105	0	0	0	1	0	0	0	0	1	1	0	0	0	0	0
106	0	0	0	0	1	0	0	0	0	0	1	1	0	0	0
56	0	0	0	0	0	1	0	0	0	0	1	1	1	1	1
58	0	0	0	0	0	0	1	0	0	0	1	1	1	1	0
107	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1

After the rows of B_{ar} containing edges e, f, and q have been deleted from B_{ar}, the following rows remain: 62, 64, 66, 68, 103, 104, and 108.

Select row 64 as a Hamilton circuit for the third subgraph. Note that this row has edges p, j, and c in common with the first subgraph. Chose edges p, j, c, t, and l as the tree for this subgraph. The rows of B_{ar} that have one edge not in this tree are 64, 66, and 108. This submatrix can be put into the following form:

	g	h	s	p	j	c	t	l
64	1	0	0	1	1	1	1	1
66	0	1	0	1	1	1	1	0
108	0	0	1	0	0	0	1	1

It is seen that this submatrix meets the criterion for realizability and the tree is a path of the subgraph consisting of the edges p, j, c, t and l in that order. It is further noted that this submatrix and the first submatrix have their common edges appearing in the same order.

When the rows of B_{ar} containing edges g, h, and s are deleted, B_{ar} is a null matrix and there are v - 1 edges in the tree. The tree can be drawn as:

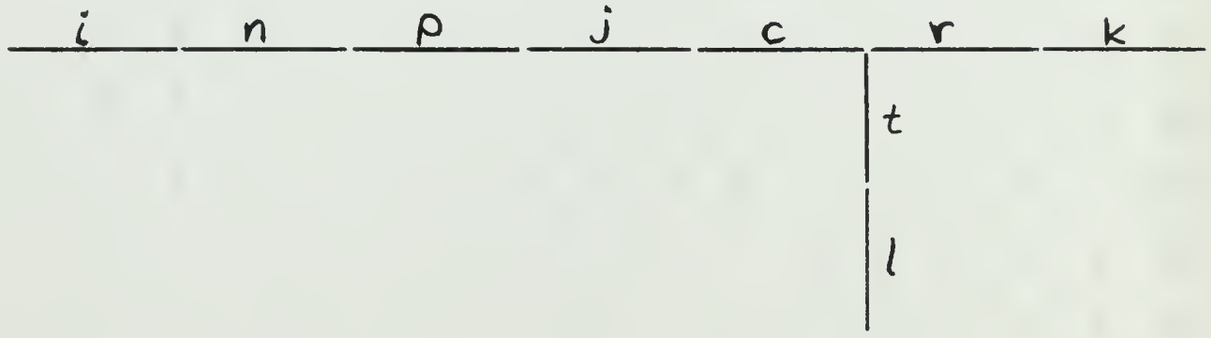

Figure 3

6.3 Example 2.

In this example, the principles of series combination and parallel combination are illustrated. The given circuit matrix can be reduced to the following form by Jordan's elimination method.

a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p	q	r	s	t	u	v	w	x
1	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0	1	1	1	0	1
0	1	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1	1	0	1
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0
0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0
0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	0

The third and fourth rows imply that edges c and d are parallel edges, replace them with edge c'. The seventh and eighth rows imply that edges g and h are parallel edges, replace them with edge g'. The tenth and eleventh rows imply that edges j and k are parallel edges, replace them with edge j'.

Since edge a or o does not appear in a row without the other also appearing, edges a and o are series edges, replace them with edge a'. The same argument holds for edges e and s as well as for edges t and x. Replace edges e and s with edge e'. Replace edges t and x with edge t'.

This matrix can be put into the following form:

a'	b	c'	e'	f	g'	i	j'	l	m	n	p	q	r	t'	u	v	w
1	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1	1	0
0	1	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0	1	1	0	1	1	1	0
0	0	0	0	1	0	0	0	0	0	0	1	1	1	0	0	0	0
0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	0	0	0
0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	1
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1

There are no series edges or parallel edges in the graph corresponding to this circuit matrix. Modulo-2 addition of all combinations of the rows of this circuit matrix, after elimination of all edge-disjoing unions of circuits, will yield B_{ar}. B_{ar} is shown in figure 4.

Select row 19 as a Hamilton circuit for the first subgraph. The tree for this subgraph is chosen to be edges c', e', f, g', l, n, and q. The rows of B_{ar} that have exactly one edge not in this tree are 19, 33, 51, 52, and 54. This submatrix can be put into the following form:

	a'	b	m	p	r	l	c'	n	q	g'	f	e'
19	1	0	0	0	0	1	1	1	1	1	1	1
33	0	1	0	0	0	1	1	0	0	0	0	0
51	0	0	1	0	0	0	1	1	0	0	0	0
52	0	0	0	1	0	0	0	0	0	1	1	0
54	0	0	0	0	1	0	0	0	1	1	0	0

It is seen that this submatrix meets the criterion for realizability and the tree is a path of the subgraph consisting of the edges

l, c', n, q, g', f, and e' in that order. After the rows of B_{ar} containing edges a', b, m, p, and r have been deleted, the following rows remain in B_{ar}: 43, 44, 45, 46, 55, 56, and 57.

	a'	b	c'	e'	f	g'	i	j'	l	m	n	p	q	r	t'	u	v	w
1	1	1	1	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0
2	1	1	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0
3	1	1	1	1	1	1	0	0	0	0	0	0	1	0	0	0	0	0
4	1	1	1	1	0	1	0	0	0	0	0	1	0	1	0	0	0	0
5	1	1	1	0	0	0	1	0	0	0	0	0	0	0	1	0	0	1
6	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0
7	1	1	1	0	0	0	1	1	0	0	0	0	0	0	1	0	1	0
8	1	1	1	0	0	0	0	1	0	0	0	0	0	0	1	1	0	1
9	1	1	0	1	0	0	0	0	0	0	1	1	1	0	0	0	0	0
10	1	1	0	1	1	0	0	0	0	0	1	0	0	1	0	0	0	0
11	1	1	0	1	1	1	0	0	0	0	1	0	1	0	0	0	0	0
12	1	1	0	1	0	1	0	0	0	0	1	1	0	1	0	0	0	0
13	1	1	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	1
14	1	1	0	0	0	0	0	0	0	0	1	0	0	0	1	1	1	0
15	1	1	0	0	0	0	1	1	0	0	1	0	0	0	1	0	1	0
16	1	1	0	0	0	0	0	1	0	0	1	0	0	0	1	1	0	1
17	1	0	1	1	0	0	0	0	1	0	1	1	1	0	0	0	0	0
18	1	0	1	1	1	0	0	0	1	0	1	0	0	1	0	0	0	0
19	1	0	1	1	1	1	0	0	1	0	1	0	1	0	0	0	0	0
20	1	0	1	1	0	1	0	0	1	0	1	1	0	1	0	0	0	0
21	1	0	1	0	0	0	1	0	1	0	1	0	0	0	1	0	0	1
22	1	0	1	0	0	0	0	0	1	0	1	0	0	0	1	1	1	0
23	1	0	1	0	0	0	1	1	1	0	1	0	0	0	1	0	1	0
24	1	0	1	0	0	0	0	1	1	0	1	0	0	0	1	1	0	1
25	1	0	0	1	0	0	0	0	1	1	0	1	1	0	0	0	0	0
26	1	0	0	1	1	0	0	0	1	1	0	0	0	1	0	0	0	0

Figure 4

	a'	b	c'	e'	f	g'	i	j'	l	m	n	p	q	r	t'	u	v	w
27	1	0	0	1	1	1	0	0	1	1	0	0	1	0	0	0	0	0
28	1	0	0	1	0	1	0	0	1	1	0	1	0	1	0	0	0	0
29	1	0	0	0	0	0	1	0	1	1	0	0	0	0	1	0	0	1
30	1	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1	1	0
31	1	0	0	0	0	0	1	1	1	1	0	0	0	0	1	0	1	0
32	1	0	0	0	0	0	0	1	1	1	0	0	0	0	1	1	0	1
33	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
34	0	1	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0
35	0	0	0	1	0	0	1	0	0	0	0	1	1	0	1	0	0	1
36	0	0	0	1	0	0	0	0	0	0	0	1	1	0	1	1	1	0
37	0	0	0	1	0	0	1	1	0	0	0	1	1	0	1	0	1	0
38	0	0	0	1	0	0	0	1	0	0	0	1	1	0	1	1	0	1
39	0	0	0	1	1	0	1	0	0	0	0	0	0	1	1	0	0	1
40	0	0	0	1	1	0	0	0	0	0	0	0	0	1	1	1	1	0
41	0	0	0	1	1	0	1	1	0	0	0	0	0	1	1	0	1	0
42	0	0	0	1	1	0	0	1	0	0	0	0	0	1	1	1	0	1
43	0	0	0	1	1	1	1	0	0	0	0	0	1	0	1	0	0	1
44	0	0	0	1	1	1	0	0	0	0	0	0	1	0	1	1	1	0
45	0	0	0	1	1	1	1	1	0	0	0	0	1	0	1	0	1	0
46	0	0	0	1	1	1	0	1	0	0	0	0	1	0	1	1	0	1
47	0	0	0	1	0	1	1	0	0	0	0	1	0	1	1	0	0	1
48	0	0	0	1	0	1	0	0	0	0	0	1	0	1	1	1	1	0
49	0	0	0	1	0	1	1	1	0	0	0	1	0	1	1	0	1	0
50	0	0	0	1	0	1	0	1	0	0	0	1	0	1	1	1	0	1
51	0	0	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0
52	0	0	0	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0

	a'	b	c'	e'	f	g'	i	j'	l	m	n	p	q	r	t'	u	v	w
53	0	0	0	0	1	0	0	0	0	0	0	1	1	1	0	0	0	0
54	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	0	0	0
55	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1	0	0
56	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	1
57	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1

Select row 45 as a Hamilton circuit for the second subgraph. The tree for this subgraph is chosen to be edges e', f, g', j', q, t', and v. The rows of B_{ar} that have exactly one edge not contained in this tree are 45, 57, and 44. This submatrix can be put into the following form:

	i	w	u	q	g'	f	e'	t'	v	j'
45	1	0	0	1	1	1	1	1	1	1
57	0	1	0	0	0	0	0	0	1	1
44	0	0	1	1	1	1	1	1	1	0

It is seen that this submatrix meets the criterion for realizability and the tree is a path of the subgraph consisting of the edges q, g', f, e', t', v, and j' in that order. It is noted that the edges common to both submatrices appear in the same order. Since the common edges appear on the ends of the paths in both subgraphs, the tree obtained when the two subgraphs are joined will be a path in the graph. The matrix for the combination of the two submatrices can be put into the following form:

	a'	b	m	p	r	i	w	u	l	c'	n	q	g'	f	e'	t'	v	j'
19	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0
33	0	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
51	0	0	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0
52	0	0	0	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0
54	0	0	0	0	1	0	0	0	0	0	0	1	1	0	0	0	0	0
45	0	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	1
57	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1
44	0	0	0	0	0	0	0	1	0	0	0	1	1	1	1	1	1	0

Since there are no rows in B_{ar} when rows containing edges i, w, and u are deleted, this matrix is a fundamental circuit matrix of the graph corresponding to B_{ar}. The tree of the graph is a path. The realized graph is shown in Fig. 5.

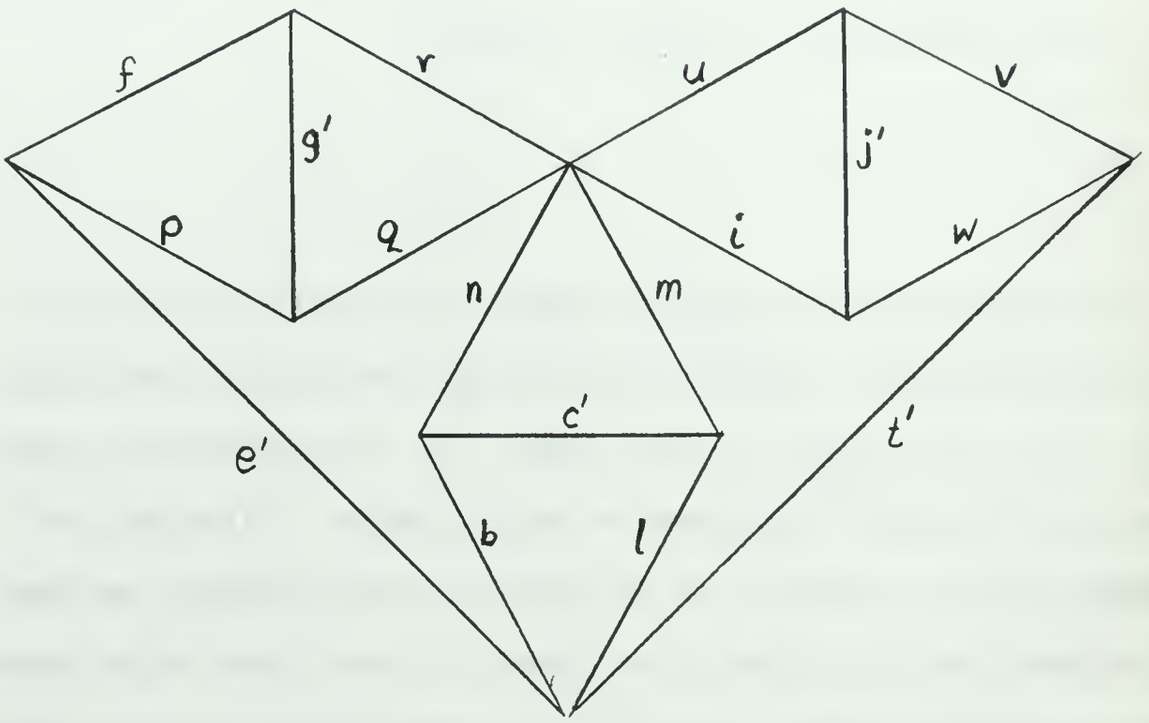

Figure 5

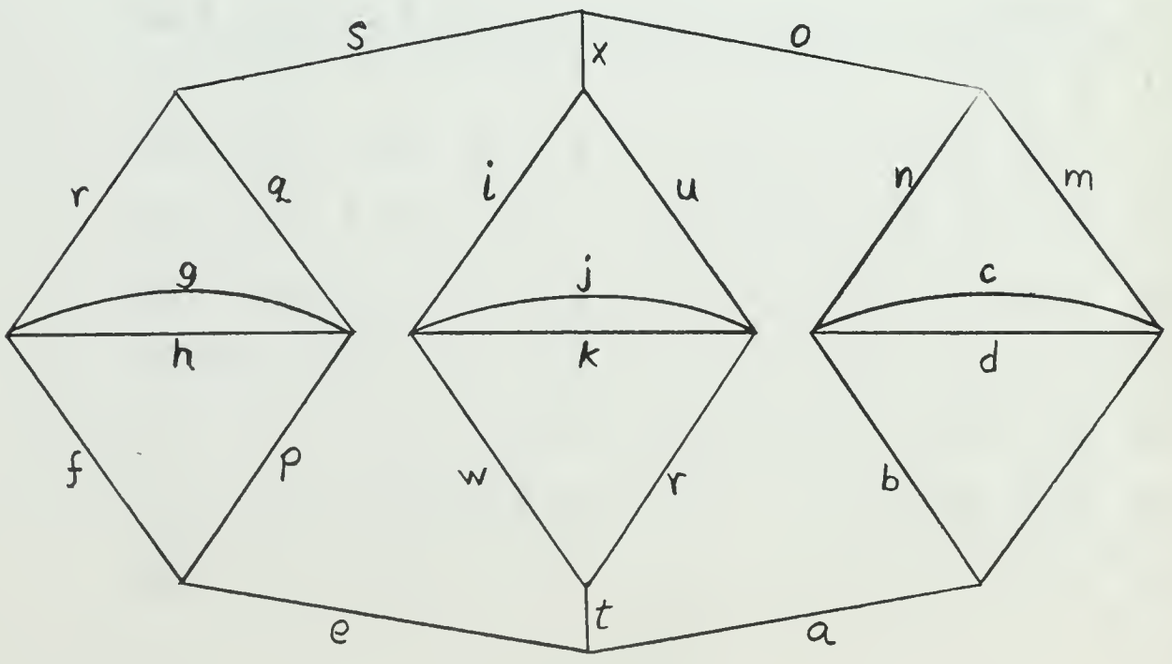

Figure 6

Figure 6 shows the completed graph after the series and parallel edges that were removed by combination are reinserted.

6.4. Example 3.

This example illustrates a given matrix that is not realizable as a circuit matrix. The following matrix is given:

a	b	c	d	e	f	g	h	i
1	1	0	1	0	0	1	0	0
1	1	0	0	1	1	0	0	0
1	1	0	0	1	0	1	1	1
1	0	1	1	0	0	0	0	1
1	0	1	0	1	0	0	1	0
0	1	1	0	0	0	1	0	1
0	1	1	0	0	1	0	1	0
0	0	0	1	1	0	0	1	1
0	0	0	1	1	1	1	0	0
0	0	0	0	0	1	1	1	1
0	1	0	0	1	0	0	1	1

Using Jordan's elimination method, this matrix can be reduced to the following form:

a	b	c	d	f	e	g	h	i
1	0	0	0	0	0	1	0	0
0	1	0	0	0	1	0	1	1
0	0	1	0	0	1	1	1	0
0	0	0	1	0	1	0	1	1
0	0	0	0	1	0	1	1	1

The first row implies that edges a and g are parallel edges, replace them with edge a'. The second and fourth rows imply that edges b and d are parallel edges, replace them with edge b'.

The resulting matrix can be put into the following form:

a'	b'	c	f	e	h	i
1	0	0	1	0	1	1
0	1	0	0	1	1	1
0	0	1	1	1	0	1

The number of vertices in the graph corresponding to this matrix, if it exists, would be 5. The minimum number of edges required to realize a graph with five vertices is found to be eight from Theorem 1. Therefore the given matrix is not realizable as a circuit matrix.

For illustrative purposes, this fact will be ignored and the matrix will be further tested for realizability. Modulo-2 addition of all combinations of these three rows results in the following B_{ar}:

	a'	b'	c	f	e	h	i
1	1	0	0	1	0	1	1
2	0	1	0	0	1	1	1
3	0	0	1	1	1	0	1
4	1	1	0	1	1	0	0
5	1	0	1	0	1	1	0
6	0	1	1	1	0	1	0
7	1	1	1	0	0	0	1

Select row 1 as the Hamilton circuit for the first subgraph. The tree for this subgraph is chosen to be edges f, h, and i. The only row that has exactly one edge not contained in this tree is row 1. After all rows containing edge a' have been deleted, B_{ar} consists of row 2, 3, and 6.

Select row 2 as the Hamilton circuit for the second subgraph. The tree for this subgraph is chosen to be edges e, h, and i. The only row that has exactly one edge not contained in this subgraph is

row 2. When the rows of B_{ar} that contain edge b' have been deleted, only row 3 remains in Bar.

The first two submatrices can be combined as follows:

	a'	b'	f	h	i	e
1	1	0	1	1	1	0
2	0	1	0	1	1	1

It is seen that the common edges in the first two subgraphs can be arranged in the same order. The third subgraph must have edges f, e, and i as the tree. Since the first two subgraphs have a tree consisting of edges f, h, i, and e in that order, it is not possible for edges f, e, and i to form a path and the given matrix is not realizable as a circuit matrix.

BIBLIOGRAPHY

1. Seshu, S. "Topological Considerations in the Design of Driving Point Functions", IRE Trans. on Circuit Theory, Vol. CT-2, pp. 193-214, Oct. 1955.
2. Parker, S.R. and Lohse, H.J., "A Direct Procedure for the Synthesis of Network Graphs from a Given Fundamental Loop or Cut Set Matrix", IEEE Trans. on Circuit Theory, May 1969.
3. Fu, Y., "Realization of Circuit Matrices", IEEE Trans. on Circuit Theory, Vol. CT-12, No. 4, pp 604-607, Dec. 1965.
4. Ash, R. B. and Kim, W. H., "On Realizability of a Circuit Matrix", IRE Trans. on Circuit Theory, Vol. CT-6 pp. 219-223, June 1959.
5. Seshu, S. and Reed, M. B., "Linear Graphs and Electrical Networks", Addison-Wesley, Reading, Mass., 1961.

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13. ABSTRACT

Several procedures for the realization of a given realizable circuit matrix are reviewed and the techniques discussed. A new method for the realization of a given circuit matrix is introduced. The procedure also introduce a positive test to determine if the given matrix is realizable as a circuit matrix.

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